

FIG. 1A
 PRIOR ART

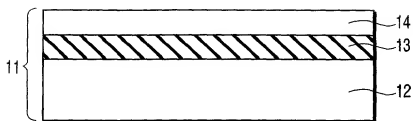


FIG. 1B
 PRIOR ART



FIG. 1C
 PRIOR ART

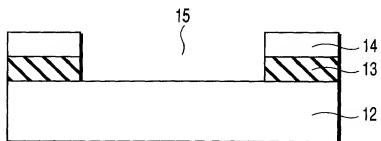


FIG. 1D
 PRIOR ART

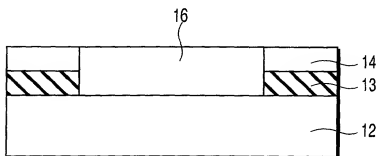


FIG. 2
 PRIOR ART

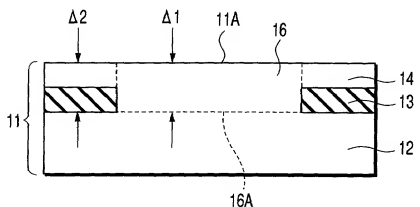


FIG. 3
PRIOR ART

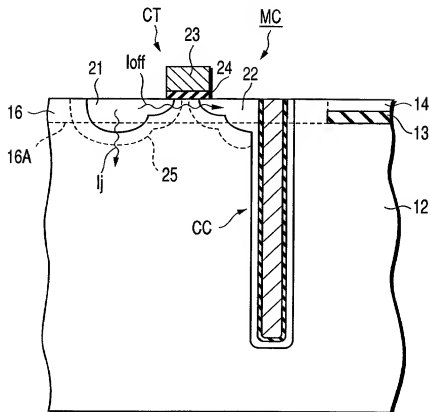
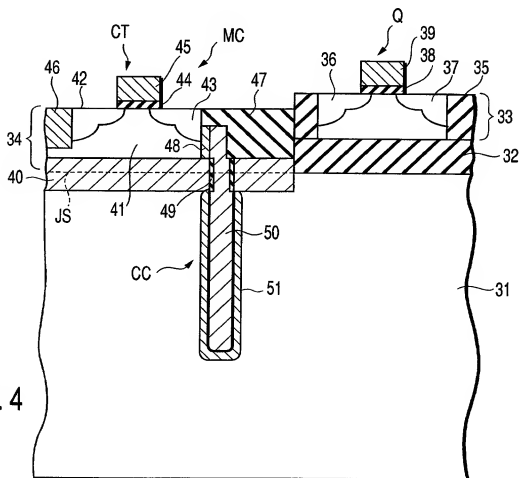


FIG. 4



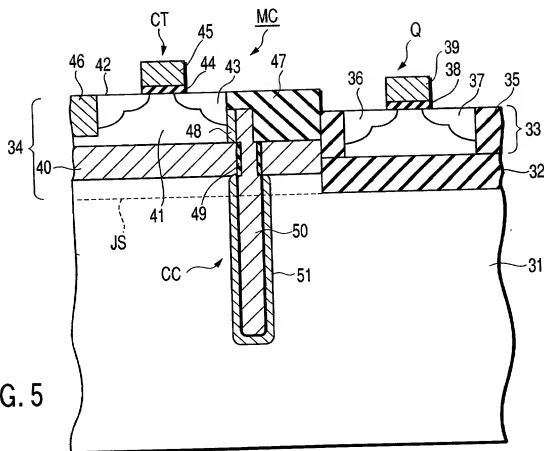


FIG. 5

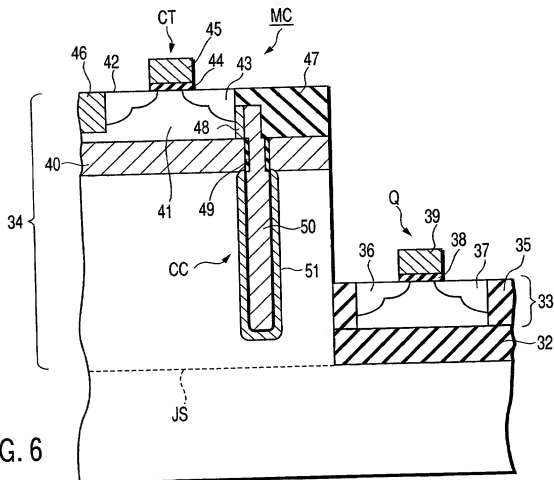


FIG. 6

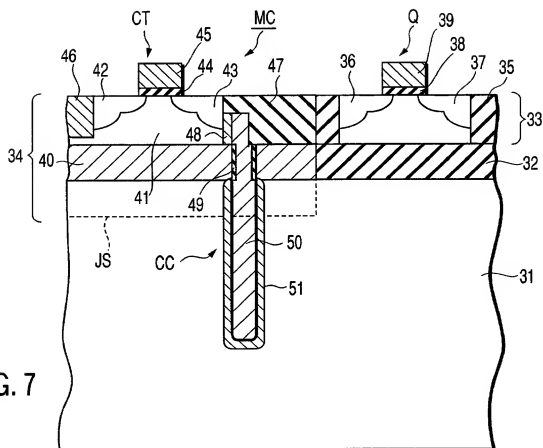


FIG. 7

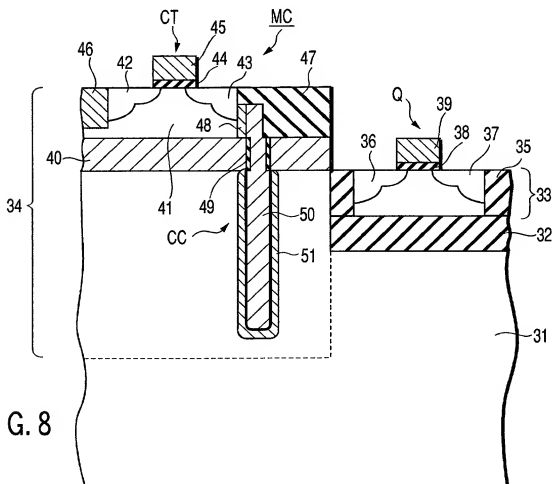


FIG. 8

FIG. 9A

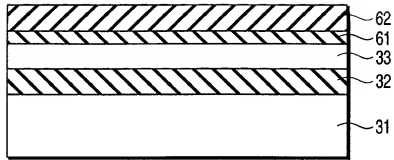


FIG. 9B

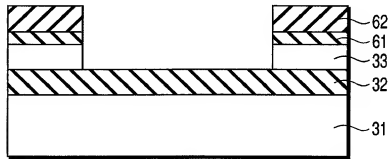


FIG. 9C

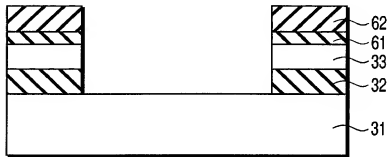


FIG. 9D

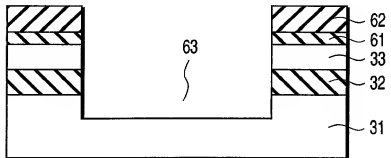


FIG. 9E

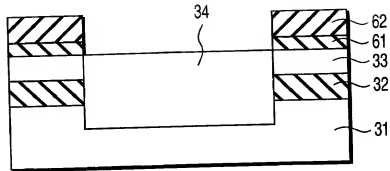


FIG. 10

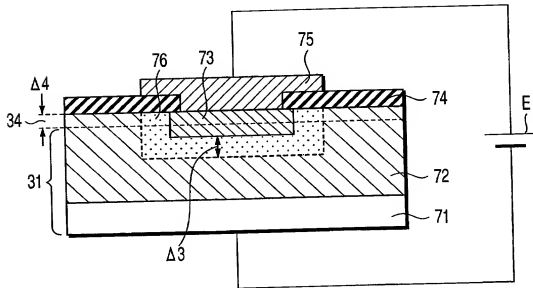
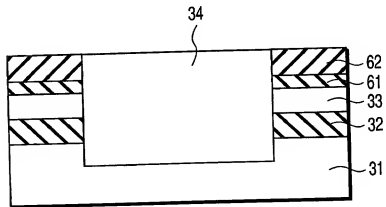


FIG. 11

20250414.02410

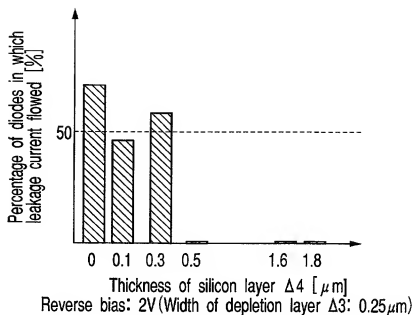


FIG. 12

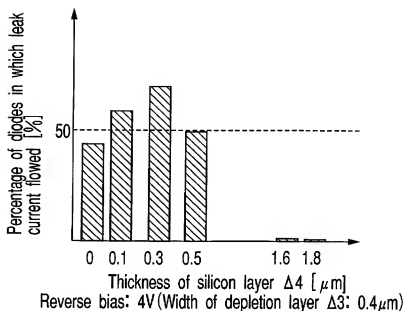


FIG. 13

- RE1: Leakage current when thickness of silicon layer is set at 0, 0.1, 0.3 μm
 RE2: Leakage current when thickness of silicon layer is set at 0.5 μm
 RE3: Leakage current in this embodiment (when thickness of silicon layer is set at 1.6, 1.8 μm)

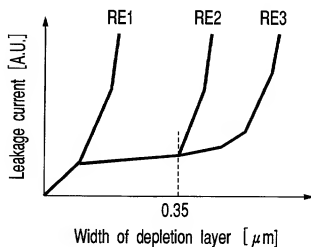


FIG. 14

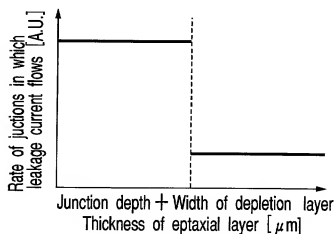


FIG. 15

FIG. 16A

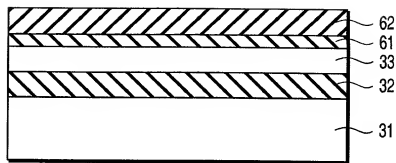


FIG. 16B

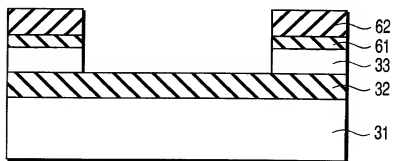


FIG. 16C

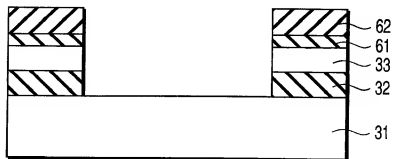


FIG. 16D

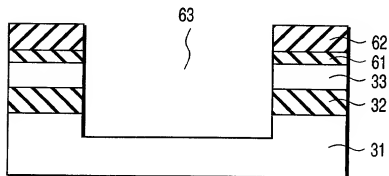


FIG. 16E

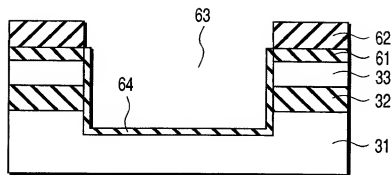


FIG. 16F

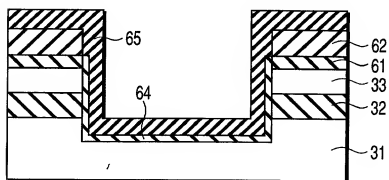


FIG. 16G

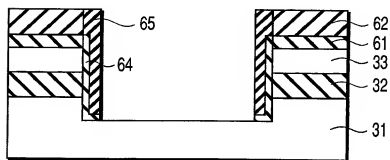


FIG. 16H

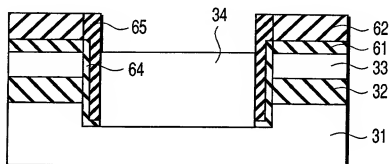


FIG. 17

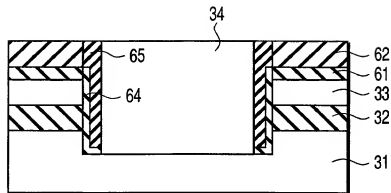


FIG. 18A

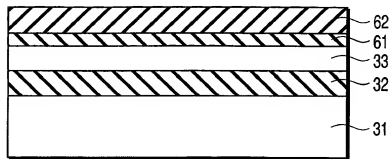


FIG. 18B

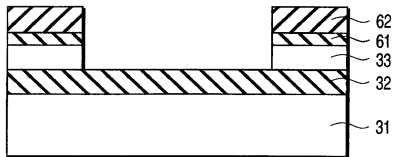


FIG. 18C

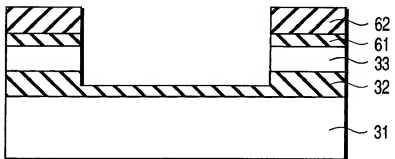


FIG. 18D

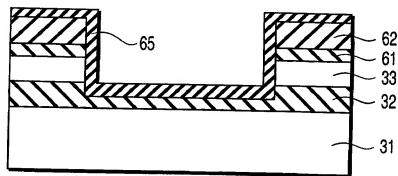


FIG. 18E

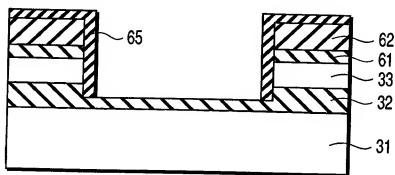


FIG. 18F

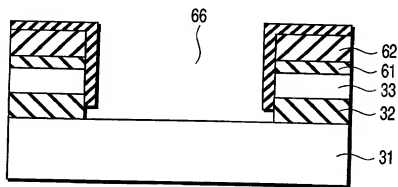


FIG. 18G

